Failure diagnostics for 3D system integration technologies in microelectronics

Frank Altmann[1], Christian Schmidt[1], Sebastian Brand[1], Peter Czurratis[2], Matthias Petzold[1*]
[1]) Fraunhofer Institute for Mechanics of Materials IWM Walter-Hülse-Straße 1, D-06120 Halle (Saale), Germany
[2]) PVA Tepla Analytical Systems GmbH, Gartenstraße 133, D-73430 Aalen, Germany
* Matthias.Petzold@iwmh.fraunhofer.de

Recently, technologies for 3D integration of semiconductor devices have attracted increasing attention, rapidly. A variety of advanced processing steps is required by these innovative concepts, involving improved chip thinning and the formation of Through Silicon Via (TSV) which is typically achieved by reactive ion etching. Furthermore, different wafer-to wafer and chip-to wafer bonding approaches have to be employed for 3D assembly and interconnect formation. Applicable technologies range from direct bonding or thermocompression Cu bonding, up to interconnect formation based on micro solder bumps, microinserts, or solid-liquid interdiffusion. However, the complexity of 3D high-density integration with respect to novel designs, processes, materials and reduced testability due to buried interconnects pose severe challenges to the techniques and tools applied for material characterization and failure analysis.

In this paper, a novel methodical approach for failure analysis on 3D integrated TSV samples is introduced. It allows to link non-destructive fault localization with efficient and accurate target preparation as well as with adapted defect characterization, forming a subsequent analysis workflow. The concept combines the application of improved Lock-In Thermography (LIT), specifically adapted Scanning Acoustic Microscopy (SAM) and new high rate-Focused Ion Beam (FIB) techniques. In the first part of the paper, it is demonstrated that LIT provides a superior potential for analyzing electrically defective interconnects inside vertically stacked silicon chips including the TSVs. LIT may not only be applied to isolate failing vertical interconnects in high density TSV arrays, but simultaneously enables also a precise 3D defect localization inside a single TSV or a stack of bonded Si components. It is shown that the achieved spatial and depth resolution is significantly improved compared to alternative fault isolation methods. Particularly in case of MEMS 3D integration, e.g. based on direct bonding, related interface defects can also be investigated by SAM. With respect to 3D integration applications, the potential of recent SAM improvements applying specifically adapted hardware and custom-made signal processing algorithms will be discussed. Examples of SAM-based failure detection techniques for the application in 3D integration are demonstrated.

Typically, identified defects traced by either LIT or SAM require subsequent cross section target preparation for further failure analysis. It is shown that novel high-efficient Focused Ion Beam (FIB) milling techniques, based on enhanced ion beam currents combined with improved supporting etching chemistry, or utilizing additional plasma sources, provide excellent erosion rates for silicon components. As a consequence, FIB milling through the complete wafer up to several hundreds of micrometers in depth becomes possible. This enables rapid and precise access to the fault sites previously localized by LIT and SAM in the wafer bonded interfaces, in the buried interconnects, or inside a TSV. As a result, high resolution electron microscopy and material diagnostics could be applied for 3D integration specimens with significantly improved throughput and efficiency. Thus, the comprehensive failure diagnostics approach developed here can support an effective process step development for current 3D integrated devices. In addition, it may contribute to improve the reliability properties of the assembled complex devices and systems.